Radu Teodorescu
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Academic Appointments

- 2021 – Present. Professor, The Ohio State University, Computer Science and Engineering, United States
- 2014 – 2021. Associate Professor, The Ohio State University, Computer Science and Engineering, United States
- 2008 - 2014. Assistant Professor, The Ohio State University, Computer Science and Engineering, United States
- 2002 - 2008. Graduate Research Assistant, University of Illinois, Computer Science, United States

Other Appointments

- 2006. Graduate Intern, Intel Research, Pittsburgh

Degrees

- 2002 - 2008. PhD, University of Illinois, Computer Science.
- 2002 - 2005. MS, University of Illinois, Computer Science.
- 1997 - 2002. BS, Technical University of Cluj-Napoca, Computer Science.

Awards

- 2023 Best Paper Award for 2022, IEEE Computer Architecture Letters (CAL), Editorial Board
- 2021 OSU CSE Department Teaching Award
- 2019 Best Paper Award for 2019, IEEE Computer Architecture Letters (CAL), Editorial Board
- 2019 IEEE MICRO Top Picks from Architecture Conferences in 2019, Honorable Mention, Top Picks Program Committee
- 2016 IEEE MICRO Top Picks from Architecture Conferences in 2015, Honorable Mention, IEEE
- 2015 Nominated for Best Paper Award at HPCA 2016. Program Committee
- 2014 Lumley Research Award, College of Engineering, The Ohio State University
- 2013 Early Career Award, National Science Foundation
- 2010 Best Paper Award at SBAC-PAD 2010, Program Committee of SBAC-PAD
- 2008 W. J. Poppelbaum Award, University of Illinois at Urbana Champaign
- 2007 Intel Foundation Ph.D. Fellowship, Intel Foundation
- 2006 David J. Kuck Outstanding Master's Thesis Award, University of Illinois at Urbana Champaign

Graduate Students: Number Completed and Number Current

Category	Current	Graduated
i) Doctoral Students (Dissertation Advisor)	4	10

Doctoral Students (Dissertation Advisor)

2019 - Present	Ghaniyoun Moein, Dissertation Advisor. N/A. The Ohio State University. Current Student.
2018 – 2024	Majumdar Saikat, Dissertation Advisor. N/A. The Ohio State University. Current Student.
2014-2020 2019-2021	Mohammad Samavatian, Dissertation Advisor. The Ohio State University. Current Student.
2019 - 2021	Xiaokuan Zhang, Dissertation Advisor. The Ohio State University. Graduated 2021.
2013 - 2021	Jia Guo, Dissertation Advisor. The Ohio State University. Graduated 2021.
	Barber K. Dissertation Advisor. Hardware Mitigation Techniques for Transient Execution Attacks. The Ohio State University. Graduated 2021
2013 - 2019	Zhou L. Dissertation Advisor. Parallel Processing Systems for Data and Computation Efficiency with Applications to Graph Computing and Machine Learning. The Ohio State University. Graduated: 2019. Current Positions: Engineer, Twitter.
2010 - 2017	Pan X. Dissertation Advisor. Designing Future Low-Power and Secure Processors with Non-Volatile Memory. The Ohio State University. Graduated: 2017. Current Positions: Senior Engineer, Qualcomm.
2010 - 2016	Sedaghati N. Co-Advisor. Performance Optimization of Memory-Bound Programs on Data Parallel Accelerators. The Ohio State University. Graduated: 2016. Current Positions: Research Engineer, Imagination Technologies.
2011 - 2016	Bacha A. Dissertation Advisor. Harnessing On-chip Error Correction for Energy Efficiency and Security. The Ohio State University. Graduated: 2016. Current Positions: Assistant Professor, University of Michigan, Dearborn.
2010 - 2015	Thomas R. Dissertation Advisor. Architectural Solutions For Mitigating Voltage Noise in GPUs. The Ohio State University. Graduated: 2015. Current Positions: Power and Performance Engineer, Intel.
2009 - 2012	Miller T. Dissertation Advisor. Architectural Solutions for Low-power, Low-voltage, and Unreliable Silicon Devices. The Ohio State University. Graduated: 2012. Current Positions: Assistant Professor, SUNY Binghampton.

Noteworthy accomplishments of graduate students:

Timothy Miller, my first PhD graduate, has published 8 papers during his PhD including several in the best venues in our field (ISCA, MICRO, HPCA). He received the OSU CSE Department's Research Award in 2012. He now holds a tenure-track Assistant Professor position in the Computer Science Department at SUNY Binghamton. He won the National Science Foundation CAREER award in 2014.

Renji Thomas, my second PhD graduate has authored and co-authored multiple publications in top venues, including HPCA 2016 and ISPASS 2016. His HPCA 2016 paper was nominated for Best Paper Award. Renji is now a researcher with Intel Hillsboro.

Anys Bacha, my third PhD graduate has published in the best venues in the field, including 1 paper in ISCA 2013 and 2 papers in MICRO 2014 and 2015. His MICRO 2015 paper was selected as a IEEE MICRO 2015 Top Picks

from architecture conferences Honorable Mention. He received the OSU CSE Department's Research Award in 2016. He is now an Assistant Professor at University of Michigan, Dearborn

Kristin Barber, my seventh PhD student won a Best Paper Award for her paper “Isolating Speculative Data to Prevent Transient Execution Attacks” published in Computer Architecture Letters, from the CAL Editorial Board. She also won an IEEE MICRO Top Picks Honorable Mention, from all Architecture Conferences in 2019 for her paper “*SpecShield: Shielding speculative data from microarchitectural covert channels,* presented at the 29th International Conference on Parallel Architectures and Compilation Techniques (PACT).

Noteworthy accomplishments of undergraduate students:

Razvan Lupusoru, a senior undergraduate student, worked on a research project that involved developing a fast interface to access energy counters on Intel Core i7 microprocessors. The software he developed was used in several papers, including one published in HPCA 2012. Razvan is now working for Intel in Hillsboro, Oregon.

Anushree Dwivedi, a senior undergraduate student, worked on a research project related to power-management solutions for mobile phones. The infrastructure she developed has yielded good results and promising research directions. Anushree now works for IBM Consulting.

Alexandra Proca, a high school senior, interned in our lab in Summer 2015. She worked on building a wearable device ecosystem from available parts that included wearable sensors to detect movement, a host computer to receive and interpret movement data, wireless networking for communication with the wearable sensors and battery-based power supply. Following the internship she was admitted to North Carolina State University where she majored in Computer Science.

Conference Publications

1. Moein Ghaniyoun, Kristin Barber, Yuan Xiao, Yinqian Zhang, and Radu Teodorescu, TEESec: Pre-Silicon Vulnerability Discovery for Trusted Execution Environments, 50th Annual International Symposium on Computer Architecture (**ISCA**), June 17–21, 2023
2. Jiuqin Zhou, Yuan Xiao, Radu Teodorescu, Yinqian Zhang, ENCLYZER: Automated Analysis of Transient Data Leaks on Intel SGX, 2022 IEEE International Symposium on Secure and Private Execution Environment Design (**SEED**), September 2022
3. Saikat Majumdar, Mohammad Hossein Samavatian, Radu Teodorescu, *Characterizing Side-Channel Leakage of DNN Classifiers though Performance Counters*, IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**) (WiP), June 2022
4. Mengyuan Li, Luca Wilke , Jan Wichelmann, Thomas Eisenbarth , Radu Teodorescu, Yinqian Zhang, *A Systematic Look at Ciphertext Side Channels on AMD SEV-SNP*, 43rd IEEE Symposium on Security and Privacy (**S&P**), May 2022
5. K. Barber, M. Ghaniyoun, Y. Zhang and R. Teodorescu, *"A Pre-Silicon Approach to Discovering Microarchitectural Vulnerabilities in Security Critical Applications"* in IEEE Computer Architecture Letters (**CAL**), vol. , no. 01, pp. 9-12, January 2022.
6. Saikat Majumdar, Mohammad Hossein Samavatian, Kristin Barber, Radu Teodorescu, *Using Undervolting as an On-Device Defense Against Adversarial Machine Learning Attacks*, IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**), December 2021
7. Moein Ghaniyoun, Kristin Barber, Yinqian Zhang, Radu Teodorescu, “*IntroSpectre: A Pre-Silicon Framework for Discovery and Analysis of Transient Execution Vulnerabilities*”, International Symposium on Computer Architecture (**ISCA**), June 2021
8. Jia Guo, Gagan Agrawal, Radu Teodorescu, *Fused DSConv: Optimizing Sparse CNN Inference for Execution on Edge Devices*. IEEE/ACM International Symposium on Cluster, Cloud and Internet Computing, (**CCGrid**), May 2021

9. Mohammad Samavatian, Anys Bacha, Li Zhou, Radu Teodorescu, *RNNFast: An Accelerator for Recurrent Neural Networks Using Domain Wall Memory*, ACM Journal on Emerging Technologies in Computing Systems, (**JETC**) 2020
10. Guo, J.; Teodorescu, R.; Agrawal, G. *A Pattern-Based API for Mapping Applications to a Hierarchy of Multi-Core Devices.* Paper presented at The 20th IEEE/ACM International Symposium on Cluster, Cloud and Internet Computing (**CCGrid**) 2020
11. Xiao, Y.; Zhang, Y.; Teodorescu, R. *SPEECHMINER: A Framework for Investigating and Measuring Speculative Execution Vulnerabilities.* Paper presented at Network and Distributed System Security Symposium (**NDSS'20**), Acceptance Rate: 17.
12. Zhou, L.; Samavatian, M.H.; Bacha, A.; Majumdar, S.; Teodorescu, R. *Adaptive parallel execution of deep neural networks on heterogeneous edge devices.* Paper presented at **SEC 2019**: Proceedings of the 4th ACM/IEEE Symposium on Edge Computing, (pp. 195-208). Acceptance Rate: 33.
13. Moosavi, S.; Samavatian, M.H.; Parthasarathy, S.; Teodorescu, R.; Ramnath, R. *Accident risk prediction based on heterogeneous sparse data: New dataset and insights.* Paper presented at **SIGSPATIAL '19**: Proceedings of the 27th ACM SIGSPATIAL International Conference on Advances in Geographic Information Systems, (pp. 33-42). Acceptance Rate: 21.
14. Barber, K.; Bacha, A.; Zhou, L.; Zhang, Y.; Teodorescu, R. *SpecShield: Shielding speculative data from microarchitectural covert channels. 2019-September,* Paper presented at 29th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), (pp. 151-164). Acceptance Rate: 25.
15. Zhou, L.; Wen, H.; Teodorescu, R.; Du, D.H.C. *Distributing Deep Neural Networks with Containerized Partitions at the Edge.* Paper presented at **HotEdge '19** Workshop at 2019 USENIX Annual Technical Conference
16. Zhou, L.; Chen, R.; Xia, Y.; Teodorescu, R. *C-Graph: A highly efficient concurrent graph reachability query framework.* Paper presented at ICPP 2018: Proceedings of the 47th International Conference on Parallel Processing (**ICPP**), 2018, Acceptance Rate: 29.
17. Pan, X.; Bacha, A.; Rudolph, S.; Zhou, L.; Zhang, Y.; Teodorescu, R. *NVCool: When Non-Volatile Caches Meet Cold Boot Attacks.* Paper presented at 36th IEEE International Conference on Computer Design (**ICCD**), 2018, (pp. 439-448).
18. Pan, X.; Bacha, A.; Teodorescu, R. *Respin: Rethinking Near-Threshold Multiprocessor Design with Non-Volatile Memory.* Paper presented at 31st IEEE International Parallel and Distributed Processing Symposium (**IPDPS**), 2017, (pp. 265-275).
19. Dimitrios Skarlatos, Renji Thomas, Aditya Agrawal, Shibin Qin, Robert Pilawa, Ulya Karpuzcu, Radu Teodorescu, Nam Sung Kim, Josep Torrellas. *Snatch: Opportunistically Reassigning Power Allocation between Processor and Memory in 3D Stacks.* Paper presented at International Symposium on Microarchitecture (**MICRO**), 2016, (pp. 1-12).
20. Xiao, Y.; Zhang, X.; Zhang, Y.; Teodorescu, R. *One Bit Flips, One Cloud Flops: Cross-VM Row Hammer Attacks and Privilege Escalation.* Paper presented at **USENIX Security** Symposium (2016), Austin, Texas.
21. Renji Thomas, Naser Sedaghati, Radu Teodorescu. *EmerGPU: Understanding and Mitigating Resonance-Induced Voltage Noise in GPU Architectures.* Paper presented at International Symposium on Performance Analysis of Systems and Software (**ISPASS**), 2016, (pp. 1-12). Acceptance Rate: 33.
22. Renji Thomas, Kristin Barber, Naser Sedaghati, Li Zhou, Radu Teodorescu. *Core Tunneling: Variation-Aware Voltage Noise Mitigation in GPUs.* Paper presented at International Symposium on High-Performance Computer Architecture (**HPCA**), 2016, (pp. 1-12). Acceptance Rate: 22.
23. Anys Bacha and Radu Teodorescu. *Authenticache: Harnessing Cache ECC for System Authentication.* Paper presented at International Symposium on Microarchitecture (**MICRO**), 2015, (pp. 12). Acceptance Rate: 20.
24. Anys Bacha and Radu Teodorescu. *Using ECC Feedback to Guide Voltage Speculation in Low-Voltage Processors.* Paper presented at International Symposium on Microarchitecture (**MICRO**), 2014, (pp. 306-318). Acceptance Rate: 20.

25. Elango,Venmugil; Sedaghati,Naser; Rastello,Fabrice; Pouchet,Louis-Noel; Ramanujam,J; Teodorescu,Radu; Sadayappan,P. *On Using the Roofline Model with Lower Bounds on Data Movement. 11*(4). Paper presented at **HiPEAC,** 2017, (pp. 67).

26. Xiang Pan and Radu Teodorescu. *NVSleep: Using Non-Volatile Memory to Enable Fast Sleep/Wakeup of Idle Cores.* Paper presented at IEEE International Conference on Computer Design (**ICCD**), 2014, (pp. 400-407). Acceptance Rate: 25.

27. Pan, X.; Teodorescu, R. *Using STT-RAM to enable energy-efficient near-threshold chip multiprocessors.* Paper presented at Parallel Architectures and Compilation Techniques (**PACT**), 2014, (pp. 485-486). Acceptance Rate: 25.

28. Anys Bacha, Radu Teodorescu. *Dynamic Reduction of Voltage Margins by Leveraging On-chip ECC in Itanium II Processors.* Paper presented at International Symposium on Computer Architecture (**ISCA**), 2013, (pp. 297-307). Acceptance Rate: 19.

29. Timothy N. Miller, Renji Thomas, Xiang Pan, Radu Teodorescu. (2012-6-1). *VRSync: Characterizing and Eliminating Synchronization-Induced Voltage Emergencies in Many-core Processors.* Paper presented at International Symposium on Computer Architecture (**ISCA**), (pp. 1-12). Acceptance Rate: 18.

30. Timothy N. Miller, Xiang Pan, Renji Thomas, Naser Sedaghati, Radu Teodorescu. *Booster: Reactive Core Acceleration for Mitigating the Effects of Process Variation and Application Imbalance in Low-Voltage Chips.* Paper presented at International Symposium on High-Performance Computer Architecture (**HPCA**), 2012, (pp. 27-38). Acceptance Rate: 17.

31. Naser Sedaghati, Renji Thomas, Louis-Noel Pouchet, Radu Teodorescu, P. Sadayappan. *StVEC: A Vector Instruction Extension for High Performance Stencil Computation.* Paper presented at International Conference on Parallel Architectures and Compilation Techniques (**PACT**), 2011, (pp. 276-287), Acceptance Rate: 15.

32. Timothy N. Miller, Renji Thomas and Radu Teodorescu. *Mitigating the Effects of Process Variation in Ultra-low Voltage Chip Multiprocessors using Dual Supply Voltages and Half-Speed Stages.* Paper presented at Workshop on Energy-Efficient Design, in conjunction with the International Symposium on Computer Architecture (**ISCA**), 2011 (pp. 1-6).

33. Timothy N. Miller, James Dinan, Renji Thomas, Bruce Adcock and Radu Teodorescu. *Parichute: Generalized Turbocode-Based Error Correction for Near-Threshold Caches.* Paper presented at International Symposium on Microarchitecture (**MICRO**), 2010, (pp. 351-362). Acceptance Rate: 18.

34. Timothy N. Miller, Nagarjuna Surapaneni and Radu Teodorescu. (2010-10-1). *Flexible Error Protection for Energy Efficient Reliable Architectures.* Paper presented at International Symposium on Computer Architecture and High Performance Computing (**SBAC-PAD**), 2010 (pp. 1-8). Acceptance Rate: 30.

35. Timothy N. Miller, Nagarjuna Surapaneni, Radu Teodorescu and Joanne Degroat. (2009-6-1). *Flexible Redundancy in Robust Processor Architecture.* Paper presented at Workshop on Energy-Efficient Design, in conjunction with the International Symposium on Computer Architecture (**ISCA**), 2009, (pp. 1-6).

36. Radu Teodorescu and Josep Torrellas. *Variation-Aware Application Scheduling and Power Management for CMPs.* Paper presented at International Symposium on Computer Architecture (**ISCA**), 2008, (pp. 363-374), Acceptance Rate: 14.

37. Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas. (2007-12-1). *Mitigating Parameter Variation with Dynamic Fine-Grain Body Biasing.* Paper presented at International Symposium on Microarchitecture (**MICRO**), 2007, (pp. 27-42). Acceptance Rate: 21.

38. Radu Teodorescu, Brian Greskamp, Jun Nakano, Smruti R. Sarangi, Abhishek Tiwari and Josep Torrellas. (2007-6-1). *VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects.* Paper presented at Workshop on Architectural Support for Gigascale Integration in conjunction with the International Symposium on Computer Architecture (**ISCA**), 2007, (pp. 1-6).

39. Pin Zhou, Radu Teodorescu and Yuanyuan Zhou. *HARD: Hardware-Assisted Lockset-based Race Detection.* Paper presented at International Symposium on High Performance Computer Architecture (**HPCA**), 2007, (pp. 121-132). Acceptance Rate: 16.

40. S. Chen, B. Falsafi, P. B. Gibbons, M. Kozuch, T. C. Mowry, R. Teodorescu, A. Ailamaki, L. Fix, G. R. Ganger, B. Lin, S. W. Schlosser. *Log-Based Architectures for Continuous Monitoring of Deployed Code.*

Paper presented at Workshop on Architectural and System Support for Improving Software Dependability, in conjunction with International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2006,

41. Radu Teodorescu and Josep Torrellas. *The Design Complexity of Program Undo Support in a General-Purpose Processor.* Paper presented at Workshop on Complexity-Effective Design, in conjunction with the International Symposium on Computer Architecture (ISCA), 2005 (pp. 1-6).
42. Radu Teodorescu and Josep Torrellas. *Empowering Software Debugging Through Architectural Support for Program Rollback.* Paper presented at Workshop on the Evaluation of Software Defect Detection Tools, in conjunction with the Conference on Programming Language Design and Implementation (PLDI), 2005, (pp. 1-6).
43. Radu Teodorescu and Josep Torrellas. *Prototyping Architectural Support for Program Rollback Using FPGAs.* Paper presented at IEEE Symposium on Field-Programmable Custom Computing Machines (**FCCM**), 2005, (pp. 23-32). Acceptance Rate: 28.
44. Radu Teodorescu and Josep Torrellas. *Prototyping Architectural Support for Program Rollback: An Application to Software Debugging.* Paper presented at Workshop on Architecture Research Using FPGA Platforms, in conjunction with the International Symposium on High-Performance Computer Architecture (HPCA), 2005, (pp. 1-6).
45. Sergiu Nedevschi, Dan Olinic, Zoltan Gyongyi, Radu Teodorescu, Sergiu Nedevschi Jr. (2001-9-1). *Feature based retrieval of echocardiographic images using DICOM structured reporting.* Paper presented at IEEE Computers in Cardiology, (pp. 679-682).

Tech Reports

1. Shimin Chen, Babak Falsafi, Phil Gibbons, Michael Kozuch, Todd Mowry, Radu Teodorescu, A Ailamaki, L Fix, GR Ganger, SW Schlosser. (2006). Logs and lifeguards: Accelerating dynamic program monitoring (Report No. IRP-TR-06-05). [Published] Intel Research Pittsburgh, Pittsburgh.

Peer-Reviewed Journal Articles

1. Samavatian, M.H.; Bacha, A.; Zhou, L.; Teodorescu, R. RNNFast: An Accelerator for Recurrent Neural Networks Using Domain Wall Memory. *ACM Journal on Emerging Technologies in Computing Systems, 2020*
2. Barber, K.; Zhou, L.; Bacha, A.; Zhang, Y.; Teodorescu, R. (2019). Isolating Speculative Data to Prevent Transient Execution Attacks. *IEEE Computer Architecture Letters,* doi:10.1109/LCA.2019.2916328
3. Venmugil Elango, Naser Sedaghati, Fabrice Rastello, Louis-Noël Pouchet, J. Ramanujam, Radu Teodorescu, and P. Sadayappan. (2015). On Using the Roofline Model with Lower Bounds on Data Movement. *ACM Transactions on Architecture and Code Optimization (TACO), 11* (4), 23/67.
4. Timothy N. Miller, Nagarjuna Surapaneni, Radu Teodorescu. (2013). Runtime failure rate targeting for energy-efficient reliability in chip microprocessors. *Concurrency and Computation: Practice and Experience Special Issue of the Best Papers of SBAC-PAD 2010, 25* (6), 790–807.
5. Timothy N. Miller, Renji Thomas and Radu Teodorescu. (2011). Mitigating the Effects of Process Variation in Ultra-low Voltage Chip Multiprocessors using Dual Supply Voltages and Half-Speed Units. *IEEE Computer Architecture Letters (CAL), 11* (2), 45-48.
6. Smruti R. Sarangi, Brian Greskamp, Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas. (2008). VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects. *IEEE Transactions on Semiconductor Manufacturing (TSM), 21* (1), 3-13.
7. Radu Teodorescu, Jun Nakano, and Josep Torrellas. (2006). SWICH: A Prototype for Efficient Cache-Level Checkpointing and Rollback. *IEEE Micro, 26* (5), 28-40.

General Press

1. Teodorescu, R.; Panda, D.K. (2019). Message from the General Chairs. *Proceedings of the 52nd International Symposium on Microarchitecture (MICRO)*, XVI-XVII.

Presentations

International

1. Teodorescu, R. (2016). *EmerGPU: Understanding and Mitigating Resonance-Induced Voltage Noise in GPU Architectures.* International Symposium on Performance Analysis of Systems and Software (ISPASS). Lecture conducted from Uppsala, Sweden.

2. Teodorescu, R. (2016). *Core Tunneling: Variation-Aware Voltage Noise Mitigation in GPUs.* International Symposium on High-Performance Computer Architecture (HPCA). Lecture conducted from Barcelona, Spain.

3. Radu Teodorescu. (2015). *Parameter Variation at NT Voltage: The Power Efficiency vs. Resilience Tradeoff.* DARPA PERFECT PI Meeting. Lecture conducted from Austin, Texas.

4. Radu Teodorescu. (2014). *Designing Energy-Efficient Microprocessors in the Era of Unpredictable Transistors.* Technical University of Cluj-Napoca. Lecture conducted from Cluj-Napoca, Romania.

5. Radu Teodorescu. (2013). *Designing Near-Threshold Microprocessors in the Era of Unpredictable Transistors.* Workshop on Energy Secure Systems Architecture (ESSA), in conjunction with the International Symposium on Computer Architecture (ISCA). Lecture conducted from Tel Aviv, Israel.

6. Radu Teodorescu. (2013). *Dynamic Reduction of Voltage Margins by Leveraging On-chip ECC in Itanium II Processors.* International Symposium on Computer Architecture (ISCA). Lecture conducted from Tel Aviv, Israel.

7. Radu Teodorescu. (2008). *Variation-Aware Application Scheduling and Power Management for Chip Multiprocessors.* International Symposium on Computer Architecture (ISCA). Lecture conducted from Beijing, China.

8. Radu Teodorescu. (2007). *Mitigating Parameter Variation with Dynamic Fine-Grain Body Bias.* International Symposium on Microarchitecture (MICRO). Lecture conducted from Chicago, Illinois, United States.

9. Radu Teodorescu. (2005). *The Design Complexity of Program Undo Support in a General-Purpose Processor.* Workshop on Complexity-Effective Design, in conjunction with the International Symposium on Computer Architecture (ISCA). Lecture conducted from Madison, Wisconsin, United States.

10. Radu Teodorescu. (2005). *Empowering Software Debugging Through Architectural Support for Program Rollback.* Workshop on the Evaluation of Software Defect Detection Tools, in conjunction with Programming Language Design and Implementation (PLDI). Lecture conducted from Chicago, Illinois, United States.

11. Radu Teodorescu. (2005). *Prototyping Architectural Support for Program Rollback Using FPGAs.* IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM). Lecture conducted from Napa, California, United States.

National

1. Radu Teodorescu. (2014). *Voltage Speculation with ECC Feedback, Mitigating Frequency Variation.* DARPA PERFECT PI Meeting. Lecture conducted from Berkeley, California, United States.

2. Radu Teodorescu. (2014). *Boosting the Energy Efficiency of Low-Voltage Multicores.* Qualcomm. Lecture conducted from Raleigh, North Carolina, United States.

3. Radu Teodorescu. (2014). *Boosting the Energy Efficiency of Low-Voltage Multicores.* IBM TJ Watson. Lecture conducted from Westchester, New York, United States.

4. Radu Teodorescu. (2013). *Boosting the Energy Efficiency of Low-Voltage Multicores.* AMD. Lecture conducted from Austin, Texas, United States.

5. Radu Teodorescu. (2013). *Boosting the Energy Efficiency of Low-Voltage Multicores.* Intel Corp. Lecture conducted from Hillsboro, Oregon, United States.

6. Radu Teodorescu. (2013). *Parameter Variation at NT Voltage: The Power Efficiency vs. Resilience Tradeoff.* DARPA PERFECT PI Meeting. Lecture conducted from Washington, District of Columbia, United States.

7. Radu Teodorescu. (2013). *Designing Energy-Efficient Microprocessors in the Era of Unpredictable Transistors.* Department of Computer Science, Princeton University. Lecture conducted from Princeton, New Jersey, United States.

8. Radu Teodorescu. (2013). *Designing Energy-Efficient Microprocessors in the Era of Unpredictable Transistors.* Computer Engineering Seminar, University of Wisconsin-Madison. Lecture conducted from Madison, Wisconsin, United States.

9. Radu Teodorescu. (2013). *Designing Energy-Efficient Microprocessors in the Era of Unpredictable Transistors.* Computer Architecture Lab Seminar, Carnegie Mellon University. Lecture conducted from Pittsburgh, Pennsylvania, United States.

10. Radu Teodorescu. (2013). *Designing Energy-Efficient Microprocessors in the Era of Unpredictable Transistors.* Computer Architecture Seminar, Cornell University. Lecture conducted from Ithaca, New York, United States.

11. Radu Teodorescu. (2010). *Architectures for Energy Efficient Computing at Ultra-low Voltages.* Computer Architecture Seminar, Department of Computer Science, University of Illinois at Urbana Champaign. Lecture conducted from Urbana, Illinois, United States.

12. Radu Teodorescu. (2010). *Architectures for Energy Efficient Computing at Ultra-low Voltages.* Computer Architecture Lab Seminar Series, Carnegie Mellon University. Lecture conducted from Pittsburgh, Pennsylvania, United States.

13. Radu Teodorescu. (2007). *Mitigating Parameter Variation with Dynamic Fine-Grain Body Bias.* Intel PhD Fellowship Forum. Lecture conducted from Hillsboro, Oregon, United States.

Funded Research

1. 1/2023-12/2027 ACE: Evolvable Computing for Next Generation Distributed Computer Systems, SRC/DARPA JUMP 2.0 Center, $31.5M total, $1,255,274 my share
2. 8/2020 - 7/2022. STAMP: A Holistic Backward/Forward Trust Framework for Protecting Microelectronics Throughout Lifecycle. Air Force Research Laboratory. (USD 5,000,000) Research Grant. 8/2018
   PI: Khalil, Waleed; Tehranipoor, Mark
   Co-I: Asadi, Navid; Bhunia, Swarup; Bibyk, Steve; Forte, Domenic; Jin, Yier; Lee, Robert; Tawfik, Eslam; Teodorescu, Radu; Woodard, Damon; Zhang, Xinmiao
   Description: Share of the budget: $293000
3. 10/2018 - 9/2021. Detecting and Measuring Micro-architectural Side-Channel Vulnerabilities with Automated Fuzzing. Intel Corporate Research Council. (USD 300,000) Research Grant. 7/2018
   PI: Zhang, Yinqian
   Co-I: Teodorescu, Radu
   Description: Share of budget: $150,000
4. 7/2016 - 6/2021. XPS: FULL: Integrating Programming Model, Runtime, Algorithmic, and Architectural Support To Use Inexact and Heterogeneous Hardware for Scientific Computations. National Science Foundation. (USD 875,000 Total Award) Research Grant. 1/2016

PI: Agrawal, Gagan; Teodorescu, Radu
Co-I: Chou, Ching-Shan
Description: Share of budget: $428,125

5. 10/2018 - 4/2020. Secure Engineering for Trusted Systems (SETS). Air Force Research Laboratory. (USD 500,000 Total Award) Research Grant. 1/2018
   PI: Khalil, Waleed
   Co-I: Bibyk, Steven; Teodorescu, Radu
   Description: Share of budget: $97,997.
6. 2/2017 - 12/2021. Gift to Support Reseach on Graph Computing. Huawei Technologies Co. Ltd. (USD 36,290.00 Total Award) Gift. 2/2017
   PI: Teodorescu, Radu
7. 2/2013 - 1/2019. CAREER: An Integrated Treatment of Voltage Noise and Process Variability in Many-core and GPU Systems with Microarchitectural Solutions. National Science Foundation. (USD 520,000 Total Award) Research Grant. 7/2012
   PI: Teodorescu, Radu
8. 9/2012 - 5/2016. Parameter Variation at Near Threshold Voltage: The Power Efficiency versus Resilience Tradeoff. Defense Advanced Research Projects Agency. (USD 2,788,166 Total Award) Research Grant. 9/2012
   PI: Kim, Nam; Torrellas, Josep; Teodorescu, Radu
   Explanation of Role: OSU Site PI. Responsible for about half of the architectural design components for the proposed variation-tolerant near-threshold chip.
   Description: Share of the budget: $941,240.
9. 7/2011 - 6/2015. SHF: Small: GOALI: Addressing the Challenges of Parameter Variation in the Design of Ultra-Low Power Chip Multiprocessors using Near-threshold Technology. National Science Foundation. (USD 400,000 Total Award) Research Grant. 12/2010
   PI: Teodorescu, Radu
   Description: My research team is responsible for the architectural design component of the project. My co-PI is responsible for the complementary circuit design components. My team's share of budget: $264,000. Project duration: 3 years.

Service

Associate Editor

2017 - 2021. Associate Editor, *IEEE Computer Architecture Letters,* (Journal)

Program Chair

2021-2022 *Co-Chair of the Selection Committee for IEEE MICRO Top Picks from the 2021 Computer Architecture Conferences*. IEEE Micro publishes a special issue with the best papers published in the previous calendar year in Computer Architecture conferences. These papers are considered by the community to be the best-of-the-best in the field for the calendar year. The Top Picks Selection Committee chooses 12 best papers and 12 honorable mentions from eligible papers published in 2021. This year we received 109 submissions. To handle the selection process we recruited 43 Selection Committee members. We held a full-day committee meeting in January 2022. Special issue of IEEE MICRO with the 12 awarded papers will be published Summer 2022.

2021-2022 *Program Co-Chair, 36th IEEE International Parallel & Distributed Processing Symposium (IPDPS), Architecture Track*, May 30 – June 3, 2022. Together with my co-chair, we recruited 40 program committee members, handled reviews for 62 submissions to the Architecture Track and organized a 2-day program committee meeting.

2019-2020 *Program Co-Chair, Architecture Track, 49th International Conference on Parallel Processing (ICPP),*

2014 *Program Chair, Second Workshop on Near-threshold Computing (WNTC) held in conjunction with the International Symposium on Computer Architecture (ISCA) 2014*

2012 *Program Chair, Workshop on Near-threshold Computing (WNTC) held in conjunction with the International Symposium on Microarchitecture (MICRO) 2012,*

General Chair

In 2019 I served as General Co-Chair for the 52nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO) organized in Columbus in October 2019.

The event included a 3-day main conference and two days of workshops and tutorials. We had 480 attendees at the main conference and close to 200 at the 10 workshops and tutorials. The attendees were 55% graduate and undergraduate students. We had 130 attendees from Midwestern schools including Michigan, OSU, UIUC, Purdue, Wisconsin, CMU, U.Pitt, Chicago. About 20 undergraduate and graduate students from OSU volunteered to help with local arrangements. A survey of attendees conducted by the ACM SIGMICRO found 64% of respondents rating the conference as Excellent and 34% as Good, ranking as one of the top-rated editions. The poster sessions organized during the main conference received the highest scores since the survey began five years ago.

Steering Committee

2020-2022 Steering Committee Member, IEEE/ACM International Symposium on Microarchitecture (MICRO)

Program Committee Member

- 2020 - 2020. Invited Review Board, **Program Committee Member*, International Symposium on Microarchitecture (MICRO),* (Papers in Proceedings)
- 2019 - 2019. Invited Review Board, **Program Committee Member*, International Conference on Parallel Architectures and Compilation Techniques (PACT),* (Papers in Proceedings)
- 2019 - 2019. Invited Review Board, **Program Committee Member*, International Symposium on Performance Analysis of Systems and Software, (ISPASS),* (Papers in Proceedings)
- 2018 - 2018. Invited Review Board, **Program Committee Member*, International Symposium on High-Performance Computer Architecture (HPCA),* (Papers in Proceedings)
- 2018 - 2018. Invited Review Board, **Program Committee Member*, International Symposium on Microarchitecture (MICRO),* (Papers in Proceedings)
- 2018 - 2018. Invited Review Board, **Program Committee Member*, International Parallel and Distributed Processing Symposium (IPDPS),* (Papers in Proceedings)
- 2016 - 2016. Invited Review Board, **Program Committee Member* of the 28th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD),* (Papers in Proceedings)
- 2015 - 2016. Invited Review Board, **Program Committee Member* of the 2016 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS),* (Papers in Proceedings)
- 2015 - 2015. Invited Review Board, **Program Committee Member* of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC),* (Papers in Proceedings)
- 2015 - 2015. Invited Review Board, **Program Committee Member* of the IEEE International Conference on Networking, Architecture, and Storage (NES),* (Papers in Proceedings)
- 2014 - 2015. Invited Review Board, **Program Committee Member* of the International Symposium on Computer Architecture (ISCA),* (Papers in Proceedings)
- 2014 - 2014. Invited Review Board, **External Program Committee Member* of the International Symposium on Microarchitecture (MICRO),* (Papers in Proceedings)
- 2014 - 2014. Invited Review Board, **Program Committee Member* of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2015,* (Papers in Proceedings)
- 2014 - 2014. Invited Review Board, **External Program Committee Member* International Symposium on High-Performance Computer Architecture (HPCA),* (Papers in Proceedings)
- 2014 - 2014. Invited Review Board, **Program Committee Member* of the IEEE International Conference on Networking, Architecture, and Storage (NES),* (Papers in Proceedings)
- 2013 - 2013. Invited Review Board, **Program Committee Member* of the IEEE International Conference on Networking, Architecture, and Storage (NES),* (Papers in Proceedings)

- 2012 - 2012. Invited Review Board, **Program Committee Member* International Workshop on Power-aware Systems and Architectures (PASA), in conjunction with ICPP,* (Papers in Proceedings)
- 2011 - 2011. Invited Review Board, **Program Committee Member* IEEE/ACM International Symposium on Microarchitecture (MICRO),* (Papers in Proceedings)
- 2010 - 2010. Invited Review Board, **Program Committee Member* International Symposium on Computer Architecture and High-Performance Computing (SBAC-PAD),* (Papers in Proceedings)
- 2010 - 2010. Invited Review Board, **Program Committee Member* International Conference on Parallel Processing (ICPP),* (Papers in Proceedings)
- 2009 - 2009. Invited Review Board, **Program Committee Member* International Symposium on Computer Architecture and High-Performance Computing (SBAC-PAD),* (Papers in Proceedings)
- 2009 - 2009. Invited Review Board, **Program Committee Member* IEEE International Conference on High Performance Computing (HiPC),* (Papers in Proceedings)

External Program Committee Member/Reviewer

- 2017 - 2018. Invited Peer Reviewer, **External Program Committee Member* International Symposium on Computer Architecture (ISCA),*
- 2017 - 2017. Invited Peer Reviewer, **External Program Committee Member*, International Symposium on High-Performance Computer Architecture (HPCA),* (Papers in Proceedings)
- 2017 - 2017. Invited Peer Reviewer, **External Program Committee Member* International Symposium on Microarchitecture (MICRO),* (Papers in Proceedings)
- 2017 - 2017. Invited Peer Reviewer, **External Program Committee Member*, International Symposium on Computer Architecture (ISCA),* (Papers in Proceedings)
- 2016 - 2016. Invited Peer Reviewer, **External Program Committee Member* of the International Symposium on Microarchitecture (MICRO),* (Papers in Proceedings)
- 2014 - 2014. Invited Peer Reviewer, **External Program Committee Member* International Conference on Parallel Architectures and Compilation Techniques (PACT),* (Papers in Proceedings)
- 2014 - 2014. Invited Peer Reviewer, **External Program Committee Member* International Symposium on Computer Architecture (ISCA),* (Papers in Proceedings)
- 2013 - 2013. Invited Peer Reviewer, **External Program Committee Member* International Symposium On High Performance Computer Architecture (HPCA),* (Papers in Proceedings)
- 2013 - 2013. Invited Peer Reviewer, *IEEE/ACM International Symposium on Microarchitecture (MICRO),* (Papers in Proceedings)
- 2013 - 2013. Invited Peer Reviewer, *International Symposium on Computer Architecture (ISCA),* (Papers in Proceedings)
- 2012 - 2012. Invited Peer Reviewer, *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2013,* (Papers in Proceedings)
- 2012 - 2012. Invited Peer Reviewer, *International Symposium on Computer Architecture (ISCA),* (Papers in Proceedings)
- 2011 - 2011. Invited Peer Reviewer, *International Conference on Dependable Systems and Networks (DSN),* (Papers in Proceedings)
- 2011 - 2011. Invited Peer Reviewer, *Euro-Par,* (Papers in Proceedings)
- 2010 - 2010. Invited Peer Reviewer, *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS),* (Papers in Proceedings)
- 2010 - 2010. Invited Peer Reviewer, *International Symposium on Computer Architecture (ISCA),* (Papers in Proceedings)
- 2010 - 2010. Invited Peer Reviewer, *ACM SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming (PPoPP),* (Papers in Proceedings)

Journal Reviewer

- 2013 - 2013. Invited Journal Reviewer, *IEEE Computer Architecture Letters (CAL),* (Journal)
- 2013 - 2013. Invited Journal Reviewer, *ACM Computing Surveys,* (Journal)
- 2013 - 2013. Invited Journal Reviewer, *IEEE Micro,* (Journal)

- 2012 - 2012. Invited Journal Reviewer, *ACM Transactions on Architecture and Code Optimization (TACO),* (Journal)
- 2012 - 2012. Invited Journal Reviewer, *ACM Transactions on Design Automation of Electronic Systems (TOADES),* (Journal)
- 2011 - 2011. Invited Journal Reviewer, *Concurrency and Computation: Practice and Experience,* (Journal)
- 2011 - 2011. Invited Journal Reviewer, *IEEE Transactions on Computers (TC),* (Journal)
- 2011 - 2011. Invited Journal Reviewer, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI),* (Journal)
- 2011 - 2011. Invited Journal Reviewer, *IEEE Transactions on Design Automation of Electronic Systems (TODAES),* (Journal)
- 2010 - 2010. Invited Journal Reviewer, *IEEE Journal of Solid-State Circuits (JSSC),* (Journal)
- 2010 - 2010. Invited Journal Reviewer, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI),* (Journal)
- 2010 - 2010. Invited Journal Reviewer, *Journal of Parallel and Distributed Computing,* (on Network-on-Chips)(Journal)
- 2010 - 2010. Invited Journal Reviewer, *IEEE Micro,* (Hot Chips 2011)(Journal)
- 2010 - 2010. Invited Journal Reviewer, *IEEE Transactions on Computers (TC),* (Journal)
- 2010 - 2010. Invited Journal Reviewer, *ACM Transactions on Architecture and Code Optimization (TACO),* (Journal)
- 2009 - 2009. Invited Journal Reviewer, *IEEE Transactions on Computers (TC),* (Journal)

Membership Professional Societies

- 2008 - Present. Active Member. SIGARCH, SIGMICRO, Association for Computing Machinery.
- 2005 - Present. Active Member. IEEE, Institute of Electrical and Electronics Engineers.

Other service

- 2021 Panelist. Grant Review Panel. National Science Foundation.
- 2017 - 2017. Panelist. Grant Review Panel. National Science Foundation.
- 2017 - 2017. Grant Reviewer. Proposal Review. Research Grants Council (RGC) of Hong Kong.
- 2017 - 2017. Panelist. Grant Review Panel. National Science Foundation.
- 2016 - 2016. Panelist. Grant Review Panel. National Science Foundation.
- 2015 - 2015. Panelist. Grant Review Panel. National Science Foundation.
- 2013 - 2013. Panelist. Grant Review Panel. National Science Foundation.
- 2012 - 2012. Panelist. Grant Review Panel. National Science Foundation.
- 2011 - 2011. Panelist. Grant Review Panel. National Science Foundation.
- 2009 - 2009. Grant Reviewer. Proposal Review. Swiss National Science Foundation (SNSF).

Administrative Service

Department

- 2020 - Ongoing. Member, Diversity and Inclusion Committee.
- 2019 - Ongoing. **Chair**, Curriculum Committee, Columbus, United States.
- 2009 - Ongoing. Coordinator, CSE6421 Computer Architecture Course.
- 2009 - Ongoing. Member, Undergraduate Studies Committee.
- 2018 - 2019. Member, Graduate Studies Committee.

BACIS Advisor

- Since 2018 I have been serving as Faculty Advisor to the students in the Bachelor of Arts in Computer and Information Science (BACIS) program. I help them choose and navigate the Related Field and other aspects of the program. Currently I am advising more than 90 students.

Curriculum Committee Chair

- In Autumn 2019 I took over the role of Curriculum Committee Chair, responsible for managing and advancing the CSE curriculum and coordinating with other teaching units across the College and University.

College or University Committees

- 2014 - 2015. Member, College of Engineering Faculty Awards Committee.
- 2009 - 2010. Member, Computer Engineering Advisory Committee.
- 2022. Member, Institute for Cybersecurity & Digital Trust (ICDT) Director Search Committee.